REMARKS

In the Office Action, Claims 1-20 are pending and were examined. Claims 2, 10, 16 and 17 are objected. Claims 1, 3-9, 11-15 and 18-20 are rejected. Drawing Fig 5 is objected.

In this Response, no claims are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-26 in view of the following remarks.

I. Objections to Drawings

The Examiner objected to Fig 5 for failing to comply with 37 CFR 1.84(p)(4) because reference character "440" has been used to designated both "Signal Termination Device" and "PAD" in Fig 5. As suggested by the Examiner, Applicants provide a replacement sheet for FIG.5, which is amended to replace "Signal Termination Device 440" with "Signal Termination Device 430", to properly define the item number according to specification.

Accordingly, in view of Applicants' amendment to FIG. 5, Applicants request that the Examiner withdraw the objection to the drawings.

II. Double Patenting Rejection

The Examiner rejects Claims 1-20 under the provisional obviousness-type double patenting rejection as not patentably distinct from Claims 1-13 of U.S. Patent No. 6,751,782 B2 although the conflicting claims are not identical. Applicants hold in abeyance this rejection until such time as the claims on which the rejection is premised are granted.

III. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1, 3-8 and 11-14 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,739,707 to Barraclough ("Barraclough"). Applicants respectfully traverse this rejection.

Regarding Claims 1 and 11, Claims 1 and 11 disclose the following claims features which are nether expressly or inherently disclosed by Barraclough:

> a pull-up circuit coupled to a signal terminator device, the pull-up circuit including a pull-up compensation resistive element; and
>
> a pull-down circuit coupled to the signal termination device, the pull-down circuit including a pull-down compensation resistive element, wherein the pull-up and pull-down compensation resistive elements to provide analog compensation of output driver signal slew rate against device impedance variation. (Emphasis added.)

According to the Examiner, Barraclough discloses the above recited features of Claims 11 and 11 as follows:

> Since the output driver and system as taught by Barraclough comprises substantially same structure, the functionality of the pull-up and pull-down compensation resistive elements would also provide analog compensation of output driver signal slew rate against device impedance variation. (See p. 4, ¶ 3 of the Office Action mailed 09/01/2006.)

Applicants respectfully disagree with the Examiner's contention that the pull-up and pull-down compensation resistive elements, as taught by Barraclough, would also provide analog compensation of the output driver signal slew rate against device impedance variation, as recited by Claims 1 and 11. In fact, Applicants respectfully submit that Barraclough teaches the digital compensation of output drives signal slew rate rather than the analog compensation of output driver signal slew rate, as recited by Claims 1 and 11. Barraclough discloses control circuitry included for selectively activating delay circuits that control terminals of pull-down and pull-up transistors of the output buffers. (See Abstract.) Regarding the output buffers disclosed by Barraclough:

> Each output buffer provides a constant impedance voltage source illustrated as a voltage source (305,309) and an output resistor (304, 308). The output buffers also provide slew-rate limiting of the output waveform as discussed further below. Therefore, the output buffers mimic a low-pass filter so that an external low-pass filter is not necessary. (See col. 2, lines 60-66.)

Applicants respectfully submit that the constant impedance voltage source (305, 309) provided by the output buffer disclosed by Barraclough is provided by a digital delay line, for example, as shown in FIG. 4, including data input node 400 and delay stages 421, 422, 423 and

424. (See col. 3, lines 5-19.) As shown in FIGS. 5 and 6 of Barraclough, the constant impedance voltage source with slew rate limiting is provided using a delay line to either lower or increase the voltage output node 425 in steps, namely, as disclosed by Barraclough:

> At time T_0 the input data signal is low (0 volts), so that all the pull-up transistors are on and all of the pull-down transistors are off, so that output node 425 is high (V_{dd}). At time T_1 the data signal on input node 400 transitions from 0 volts to V_{dd}. Thereafter, at times T_2, T_3, T_4 and T_5, the delayed data signals appear at the outputs of delay stages 421, 422, 423 and 424, respectively. As a result, the complementary transistor pairs sequentially switch from high to low, thereby pulling the voltage on output node 425 lower in steps. (Col., 3, lines 22-31.) (Emphasis added.)

The output voltage generated by delay stages 421, 422, 423 and 424 is illustrated by Barraclough with reference to FIG. 6. As disclosed by Barraclough:

> The resulting output voltage on node 425 is shown in FIG. 6, wherein the transitions between steps occur at the corresponding times noted in FIG. 5. Similarly, when input node 400 transitions from V_{dd} to 0 volts at time T_6, the delayed data signals appear at the outputs of the above-noted delay lines at times T_7, T_8, T_9 and T_{10}. Therefore, the transistor pairs pull the output node 425 high in steps, as further illustrated in FIG. 6. Note that this step-wise technique accomplishes a smoothing of the output waveform as compared to an abrupt (square-wave) transition between V_{dd} and 0 volts (and vice-versa). The magnitude of each step (DELTA) is equal to V_{dd}/N, where N is the number of taps of the delay line. (Col. 3, lines 32-44.) (Emphasis added.)

Accordingly, by utilizing a step-wise technique, Barraclough teaches that the output waveform is smoothed in order to avoid slew rate variations by providing digital values to the delay lines comprised of stages 421, 422, 423 and 424, as shown in FIG. 4. FIG. 7 further illustrates the digital delay line taught by Barraclough to enable the output buffer to provide a constant impedance voltage source with slew rate limiting. As disclosed by Barraclough with reference to FIG. 7:

> Propagation through each section is controlled by the corresponding control line connected to the multiplexer inputs. The "0" input of a given multiplexer is selected when the corresponding control lines is at "0", and the "1" input is selected when the control line is at "1". Note that the "0" input of the left-hand multiplexer 744 is connected to a logical "1" (V_{dd}), whereas the "1" input of right-hand multiplexer 752 is connected to a logical "0" (V_{ss}). (Col., 4, lines 17-24.) (Emphasis added.)

The final output waveform disclosed by Barraclough is described as follows:

> The resultant output waveforms of the buffers at the IC output terminals are designated PIN1 and PIN2, and the waveform between the two IC terminals is designated VDIFF. Therefore, by changing the control signals in accordance with the data input, a desired output waveform (VDIFF in FIG. 8) may be obtained. (Col. 4, lines 28-34.)

The control circuit to program the delay lines taught by Barraclough to provide the constant impedance voltage source with slew rate limiting is illustrated with reference to FIG. 9. As further disclosed by Barraclough the digital values provided by the control circuit to enable the step-wise technique for outputting the waveform from the output buffer, as disclosed by Barraclough, is illustrated with reference to the Table shown in column 4, lines 48-54.

As mandated by case law, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2USPQ2d 1051, 1053 (Fed. Cir. 1987). ("Verdegaal Bros") Additionally, "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). ("Richardson")

Here, the Examiner argues that Barraclough teaches substantially same output driver, as recited by Claims 1 and 11. Applicants respectfully submit that the output driver disclosed by Barraclough is not substantially similar to the output driver recited by Claims 1 and 11. Specifically, for the reasons indicated above, Barraclough discloses a control circuit as shown in FIG. 9 of Barraclough to provide digital inputs to the various delay stages and multiplexers (744-753) to provide or implement the step-wise technique for smoothing of the output waveform provided by the output buffer, such that the output buffers implement a constant impedance voltage source with slew rate limiting.

Applicants respectfully submit that the delay logic and control circuitry for such delay logic, as disclosed by Barraclough, provides a technique for digital compensation of output driver signal slew rate rather than the analog compensation of output driver signal slew rate, as recited by Claims 1 and 11. Applicants' argument is further substantiated by the truth table shown at

column 4, lines 48-54 of Barraclough which provides a digital input device for the control circuit to enable the step-wise technique for smoothing the output waveform provided by the output buffer disclosed by Barraclough in order to provide a constant impedance voltage source with slew rate liming. as taught by Barraclough.

Therefore, Applicants respectfully submit that the Examiner is prohibited from relying on Barraclough as an anticipatory reference since Barraclough fails to disclose the identical invention recited by Claims 1 and 11 which recite an output buffer to provide analog compensation of output driver signal slew rate against device impedance variation. Richardson, supra.

Consequently, Applicants submit that the Examiner fails to establish a prima facie case of anticipation of Claims 1 and 11 since Barraclough fails to either expressly or inherently disclose the output driver recited by Claims 1 and 11 to provide analog compensation of output driver signal slew rate against device impedance variations. Verdegaal Bros, supra.

Therefore, for at least the reasons provided above, Applicants respectfully submit that Claims 1 and 11, as well as Claims 3-8 and 12-14 based on their dependencies from Claims 1 and 11, respectively, are patentable over Barraclough, as well as references of record. Consequently, Applicants respectfully request that the examiner reconsider and withdraw the §102(b) rejection of Claims 1, 3-8 and 11-14.

IV. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 9, 15 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Barraclough in view of Applicants' admitted prior art ("AAPA"). Applicants respectfully traverse this rejection.

Regarding Claims 9, 15 and 18-20, Claims 9, 15 and 18-20 depend from independent Claims 1 and 11, respectively. For at least the reasons provided above, Applicants respectfully submit that the Examiner's citing of AAPA fails to rectify the deficiencies of Barraclough to teach or suggest the analog compensation of output driver signal slew rate against device impedance variations, as recited by Claims 1 and 11. Hence, Applicants respectfully submit that

Claims 1 and 11, for at least the reasons provided above, are also patentable over the combination of Barraclough in view of AAPA.

Consequently, Claims 9, 15 and 18-20, based on their dependencies from Claims 1 and 11, respectively, are also patentable over combination of Barraclough in view of AAPA. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 9, 15 and 18-20.

V. Allowable Subject Matter

The Examiner has indicated that Claim 2, 10 and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

Applicants respectfully thank the Examiner for recognizing the allowability of Claims 2, 10 and 16-17. However, for at least the reasons provided above, Applicants respectfully submit that such claims based on their dependencies from independent Claims 1 and 11 are also patentable over Barraclough, as well as references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the objection to Claims 2, 10 and 16-17, and allow such claims, based on their dependencies from Claims 1 and 11. 6

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: October 27, 2006 By: _____
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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage on the date below, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Annie McNally 10/27/2006
Annie McNally Date